

Description

[TUNABLE ESD TRIGGER AND POWER CLAMP CIRCUIT]

BACKGROUND OF INVENTION

[0001] FIELD OF THE INVENTION

[0002] The present invention relates to the field of electrostatic discharge (ESD) and power clamp circuits; more specifically, it relates to ESD and power clamp circuits tunable to unity current gain cutoff frequency (f_T) and collector to emitter with base open breakdown voltage (BV_{ceo}).

[0003] BACKGROUND OF THE INVENTION

[0004] The manufacture of high performance bipolar transistors requires reduction of the vertical profile as well as reduction of transistor parasitics. In order to reduce the collector transit time of the carriers, the subcollector is placed close to the collector-base junction. As the base and collector regions are moved closer together, the collector-to-emitter breakdown voltage, BV_{ceo} , decreases and the

frequency response of the transistor, f_T , increases. In ESD applications, there is a need to be able to provide both a low capacitance device, or a device with a different breakdown voltage than the standard device which requires protection.

SUMMARY OF INVENTION

[0005] A first aspect of the present invention is an electrostatic discharge protection circuit, comprising: a first bipolar transistor coupled between a first circuit node and a second circuit node, the first bipolar transistor having a non-uniform subcollector region geometry, the first bipolar transistor having a different value for collector to emitter breakdown voltage than a value for collector to emitter breakdown voltage of an otherwise identical bipolar transistor having a uniform subcollector region geometry.

[0006] A second aspect of the present invention is a method of providing an electrostatic discharge protection to an integrated circuit, comprising: providing a first bipolar transistor; coupling the first bipolar transistor between a first circuit node and a second circuit node, the first bipolar transistor having a non-uniform subcollector region geometry; and selecting the non-uniform subcollector region geometry in order to tune a collector to emitter

breakdown voltage of the first bipolar transistor.

[0007] A third aspect of the present invention is a method of designing an electrostatic discharge protection circuit, comprising: providing a schematic P-cell circuit generator; providing a hierarchical P-cell layout generator; providing a graphical unit interface to the schematic P-cell circuit generator and the hierarchical P-cell layout generator; accepting a value for a collector to emitter breakdown voltage target for at least a first bipolar transistor of the electrostatic discharge protection circuit; selecting a non-uniform subcollector region geometry for the first bipolar transistor based on the value of the collector to emitter breakdown voltage target; and generating a circuit design and a layout for the electrostatic discharge protection circuit, the electrostatic discharge protection circuit containing the first bipolar transistor.

BRIEF DESCRIPTION OF DRAWINGS

[0008] The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

[0009] FIG. 1 is a plot illustrating the Johnson limit relationship

between BV_{ceo} and f_T according to the present invention;

[0010] FIG. 2A is a plan view of a first hetero-junction bipolar transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 2B is a cross-sectional view through line 2B-2B of FIG. 2A;

[0011] FIG. 3A is a plan view of a second hetero-junction bipolar transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 3B is a cross-sectional view through line 3B-3B of FIG. 3A;

[0012] FIG. 4A is a plan view of a third hetero-junction bipolar transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 4B is a cross-sectional view through line 4B-4B of FIG. 4A;

[0013] FIG. 5A is a plan view of a fourth hetero-junction bipolar transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 5B is a cross-sectional view through line 5B-5B of FIG. 5A;

[0014] FIG. 6A is a plan view of a fifth hetero-junction bipolar transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 6B is a cross-sectional view through line 6B-6B of FIG. 6A;

[0015] FIG. 7A is a plan view of a first bipolar junction transistor suitable for use in an ESD trigger and power clamp circuit

according to the present invention and FIG. 7B is a cross-sectional view through line 7B-7B of FIG. 7A;

[0016] FIG. 8A is a plan view of a second bipolar junction transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 8B is a cross-sectional view through line 8B-8B of FIG. 8A;

[0017] FIG. 9A is a plan view of a third bipolar junction transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 9B is a cross-sectional view through line 9B-9B of FIG. 9A;

[0018] FIG. 10A is a plan view of a fourth bipolar junction transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 10B is a cross-sectional view through line 10B-10B of FIG. 10A;

[0019] FIG. 11A is a plan view of a fifth bipolar junction transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 11B is a cross-sectional view through line 11B-11B of FIG. 11A;

[0020] FIG. 12A is a plot illustrating the relationship between f_T and masked subcollector pull back according to the present invention;

[0021] FIG. 13 is an ESD trigger and power clamp circuit according to a first embodiment of the present invention;

- [0022] FIG. 14 is an ESD trigger and power clamp circuit according to a second embodiment of the present invention;
- [0023] FIG. 15 is an ESD trigger and power clamp circuit according to a third embodiment of the present invention;
- [0024] FIG. 16 is an ESD trigger and power clamp circuit according to a fourth embodiment of the present invention;
- [0025] FIG. 17 is an ESD trigger and power clamp circuit according to a fifth embodiment of the present invention;
- [0026] FIG. 18 is an ESD trigger and power clamp circuit according to a sixth embodiment of the present invention;
- [0027] FIG. 19 is an ESD protection circuit according to a seventh embodiment of the present invention;
- [0028] FIG. 20 is a process flow diagram for an exemplary system for designing ESD trigger and power clamp circuits according to the present invention;
- [0029] FIG. 21 is an exemplary illustration of a graphical unit interface (GUI) screen of the ESD circuit design system illustrated in FIG. 18; and
- [0030] FIG. 22 is an exemplary ESD trigger and power clamp circuit hierarchal structure generated by the ESD circuit design system of FIG. 18.

DETAILED DESCRIPTION

- [0031] FIG. 1 is a plot illustrating the Johnson limit relationship

between BVceo and fT according to the present invention. Curve 50 is based on experimental measurement of fT and BVceo for similar size and process NPN SiGe bipolar transistors. The portion of curve 50 below about 3 volts BVceo was obtained from measurements of standard high performance NPN SiGe bipolar transistors. The portion of curve 50 above about 3 volts BVceo was obtained from measurement of from high performance devices modified according to the present invention. The curve of FIG. 1 approximates the Johnson limit equation:

[0032] $f_T \times BV_{ceo} = (E_m \times V_s) / 2\pi(1)$ where:

[0033] fT = unity current gain cutoff frequency;

[0034] BVceo = collector-emitter (base open) breakdown voltage;

[0035] Em = maximum electric field at current saturation; and

[0036] Vs = electron saturation velocity.

[0037] Curve 50 indicates that as fT increases BVceo decreases. Curve 50 indicates that for very high fT devices, BVceo may be below the value required for a device used in and ESD circuit. ESD devices typically require a BVceo higher than the operating voltage of the integrated circuit being protected. Curve 50 further indicates that devices modi-

fied for use in ESD circuits will have a lower f_T than non-modified or standard devices. However, since ESD events generally occur at frequencies lower than operating the operating frequencies of high performance devices, and operating voltages tend to decrease with increases in operating frequency, the lower f_T of modified devices is not a problem, especially for circuits designed for operation of 200 GHz or greater.

[0038] FIG. 2A is a plan view of a first hetero-junction bipolar transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 2B is a cross-sectional view through line 2B-2B of FIG. 2A. In FIG. 2A, a first SiGe bipolar transistor 100A includes an N-well 105 surrounded by deep trench isolation 110. Completely contained within the outline of N-well region 105 is a P type polysilicon base 115. Completely contained within the outline of polysilicon base 115 is a P type low-temperature epitaxial (LTE) base 120. LTE base 120 may comprise SiGe or SiGeC. SiGe (and SiGeC) bipolar transistors are examples of hetero-junction bipolar transistors. Completely contained within the outline of LTE base 120 is an upper portion 125 of N-well 105 in contact with LTE base 120. Completely contained within the out-

line of upper portion 125 of N-well 105 is an N type mono-crystalline emitter 130. The space between the heavy line rectangles 135A and 135B defines an N type masked subcollector 145 (see FIG. 2B). Masked subcollector 145 has the shape of a rectangular ring. In FIG. 2A, there is no masked subcollector 145 around emitter 130 a distance D from a plane 140 bisecting emitter 130 longitudinally. First SiGe bipolar transistor 100A also includes N type reach-thru regions 150 contacting an N-type blanket subcollector 155 (see FIG. 2B). Blanket subcollector 155 extends between deep trench isolation 110 under and in contact with N-well 105. Note only one reach-thru region 150 may be used portions of masked subcollector 145 on either side of plane 140 are integrally connected.

[0039] Turning to FIG. 2B, several structures not shown in FIG. 2A are illustrated in FIG. 2B. A shallow trench isolation 160 formed in N-well 105 defines the periphery of upper portion 125 of N-well 105. An N-doped polysilicon emitter 165 on top of polysilicon base 115 and LTE base 120 is physically separated and electrically isolated from the polysilicon base by a dielectric layer 170, a dielectric spacer 175 and a dielectric layer 180. Polysilicon emitter 165 is separated and electrically isolated from LTE base

120 by dielectric spacer 175 and dielectric layer 180.

[0040] Mono-crystalline emitter 130 is formed from a portion of polysilicon emitter 165 that is in direct physical contact with LTE base 120. Likewise LTE base 120 is formed from that portion of polysilicon base 115 in direct physical contact with N-well 105. Polysilicon base 115, LTE base 120 and polysilicon emitter 165 are formed on a top surface 185 of a bulk silicon substrate 190. Reach-thru regions 150 extend from top surface 185 of substrate 185 through masked subcollector 145 and into blanket subcollector 155. In one example, N-well 105 is an epitaxial silicon layer formed on a P type substrate. Deep trench isolation 110 may include a single dielectric layer or multiple dielectric layers or a dielectric liner with an inner polysilicon core.

[0041] In Fig. 2B, it can be seen, that D defines the distance between the maximum lateral extent of masked subcollector 145 from deep trench isolation 110 and plane 140. In other words, masked subcollector 145 extends no further than D from plane 140. The actual mask used in forming masked subcollector 145 has its edges a distance M from plane 140. The difference (M-D) is lateral out-diffusion of the ion implant used to form masked subcollector 145.

The term masked subcollector pull back refers to distance M.

[0042] The fact that masked subcollector 145 does not extend completely under upper region 125 of N-well 105, that is, masked subcollector 145 has a non-uniform geometry and non-uniform horizontal and vertical doping profiles allows a first tuning of the BV_{ceo} (and f_T) of first SiGe bipolar transistor 100A. By adjusting the distance M (and thus distance D) the doping level of the N-well between LTE base 120 and blanket subcollector 155 can be controlled so that this region can be depleted to sufficiently to give a higher BV_{ceo} (and lower f_T) than a standard device. (See FIGs. 12A and 12B which are describe infra). A standard device would be one where M is zero, where masked subcollector 145 is not present or where masked subcollector 145 is not present and blanket subcollector 155 is formed closer to LTE base 120. A second tuning of the BV_{ceo} (and f_T) of first SiGe bipolar transistor 100A may be obtained by controlling the ion species, dose and energy of the ion-implant process used to form masked subcollector 145.

[0043] FIG. 3A is a plan view of a second hetero-junction bipolar transistor suitable for use in an ESD trigger and power

clamp circuit according to the present invention and FIG. 3B is a cross-sectional view through line 3B-3B of FIG. 3A. In FIGs. 3A and 3B, a second SiGe bipolar transistor 100B is similar to first SiGe bipolar transistor 100A (see FIGs. 2A and 2B) except that masked subcollectors 145A and 145B in FIG. 3B which are seen in FIG. 3A to be dual stripes defined by the heavy line rectangles 135C and 135D are not integral with one another. Thus it is necessary for there to be two separate reach-thru regions 150, one contacting each masked subcollector 145A and 145B.

[0044] FIG. 4A is a plan view of a third hetero-junction bipolar transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 4B is a cross-sectional view through line 4B-4B of FIG. 4A. In FIGs. 4A and 4B, a third SiGe bipolar transistor 100C is similar to second SiGe bipolar transistor 100B (see FIGs. 3A and 3B) except that there is only one masked subcollector 145C in FIG. 4B which is seen in FIG. 4A to be a single stripe defined by the heavy line rectangle 135E. Thus it is necessary for there to be only one reach-thru region 150 contacting masked subcollector 145C.

[0045] FIG. 5A is a plan view of a fourth hetero-junction bipolar transistor suitable for use in an ESD trigger and power

clamp circuit according to the present invention and FIG. 5B is a cross-sectional view through line 5B-5B of FIG. 5A. In FIGs. 5A and 5B, a fourth SiGe bipolar transistor 100D is similar to first SiGe bipolar transistor 100A (see FIGs. 2A and 2B) except that substrate 190A is an silicon-on-insulator (SOI) substrate which includes a buried oxide (BOX) layer 190B. There is no blanket subcollector 155 (see FIG. 2B).

[0046] It should be noted that the second and third SiGe bipolar transistors 100B and 100C may also be fabricated on an SOI substrate instead of the bulk substrate illustrated in FIGs. 3B and 4B respectively.

[0047] FIG. 6A is a plan view of a fifth hetero-junction SiGe bipolar transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 6B is a cross-sectional view through line 6B-6B of FIG. 6A. In FIGs. 6A and 6B, a fifth SiGe bipolar transistor 100E is similar to first SiGe bipolar transistor 100A (see FIGs. 2A and 2B) except that in FIGs. 6A and 6B a tuning ion implant 195 has been performed to change the doping level between the upper region 125 of N-well 125 and masked subcollector 145. Thus a third tuning of the BV_{ceo} (and f_T) of fifth SiGe bipolar transistor 100E may be obtained

by controlling the ion species, dose and energy of ion-implant 195.

[0048] It should be noted that the second, third and fourth SiGe bipolar transistors 100B (see FIGs. 3A and 3B), 100C (see FIGs. 4A and 4B) and 100D (see FIGs. 5A and 5B) may also employ a tuning ion implant as illustrated in FIG. 6B and described supra.

[0049] FIG. 7A is a plan view of a first bipolar junction transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 7B is a cross-sectional view through line 7B-7B of FIG. 7A. In FIG. 7A, a first bipolar junction transistor 200A includes an N-well 205 surrounded by deep trench isolation 210. Completely contained within the outline of N-well region 205 is a P type base 220. Completely contained within the outline of base is an N type emitter 230. The space between the heavy line rectangles 235A and 235B defines an N type masked subcollector 245 (see FIG. 7B). Masked subcollector 245 has the shape of a rectangular ring. In FIG. 7A, there is no masked subcollector 245 around emitter 230 a distance D from a plane 240 bisecting emitter 230 longitudinally. First bipolar junction transistor 200A also includes N type reach-thru regions 250 contacting an N-

type blanket subcollector 255 (see FIG. 7B). Blanket subcollector 255 extends between deep trench isolation 210 under and in contact with N-well 205. Note only one reach-thru region 250 may be used portions of masked subcollector 245 on either side of plane 240 are integrally connected.

[0050] Turning to FIG. 7B, several structures not shown in FIG. 7A are illustrated in FIG. B. A shallow trench isolation 260 formed in N-well 205 defines the periphery of base 220. Emitter 230 is formed within base 220.

[0051] Reach-thru regions 250 extend from top surface 285 of a substrate 290 through masked subcollector 245 and into blanket subcollector 255. In one example, N-well 205 is an epitaxial silicon layer formed on a P type substrate. Deep trench isolation 210 may include a single dielectric layer or multiple dielectric layers or a dielectric liner with an inner polysilicon core.

[0052] In Fig. 7B, it can be seen, that D defines the distance between the maximum lateral extent of masked subcollector 245 from deep trench isolation 210 and plane 240. In other words, masked subcollector 245 extends no further than D from plane 240. The actual mask used in forming masked subcollector 245 has its edges a distance M from

plane 240. The difference (M-D) is lateral out-diffusion of the ion implant used to form masked subcollector 245. The term masked subcollector pull back refers to distance M.

[0053] The fact that masked subcollector 245 does not extend completely under base 220, that is, has a non-uniform geometry and non-uniform horizontal and vertical doping profiles allows a first tuning of the BVceo (and fT) of first bipolar junction transistor 200A. By adjusting the distance M (and thus distance D) the doping level of the N-well between base 220 and blanket subcollector 255 can be controlled so that this region can be depleted sufficiently to give a higher BVceo (and lower fT) than a standard device. A standard device would be one where M is zero, where masked subcollector 245 is not present or where masked subcollector 245 is not present and blanket subcollector 255 is formed closer to base 215. A second tuning of the BVceo (and fT) of first bipolar junction transistor 200A may be obtained by controlling the ion species, dose and energy of the ion-implant process used to form masked subcollector 245.

[0054] FIG. 8A is a plan view of a second bipolar junction transistor suitable for use in an ESD trigger and power clamp cir-

cuit according to the present invention and FIG. 8B is a cross-sectional view through line 8B-8B of FIG. 8A. In FIGs. 8A and 8B, a second bipolar junction transistor 200B is similar to first bipolar junction transistor 200A (see FIGs. 7A and 7B) except that masked subcollectors 245A and 245B in FIG. 7B which are seen in FIG. 7A to be dual stripes defined by the heavy line rectangles 235C and 235D are not integral with one another. Thus it is necessary for there to be two separate reach-thru regions 250, one contacting each masked subcollector 245A and 245B.

[0055] FIG. 9A is a plan view of a third bipolar junction transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 9B is a cross-sectional view through line 9B-9B of FIG. 9A. In FIGs. 9A and 9B, a third bipolar junction transistor 200C is similar to second bipolar junction transistor 200B (see FIGs. 8A and 8B) except that there is only one masked subcollector 245C in FIG. 9B which is seen in FIG. 9A to be a stripe defined by the heavy line rectangle 235E. Thus it is necessary for there to be only one reach-thru region 250 contacting masked subcollector 245C.

[0056] FIG. 10A is a plan view of a fourth bipolar junction transistor suitable for use in an ESD trigger and power clamp

circuit according to the present invention and FIG. 10B is a cross-sectional view through line 10B–10B of FIG. 10A. In FIGs. 10A and 10B, a fourth bipolar junction transistor 200D is similar to first bipolar junction transistor 200A (see FIGs. 7A and 7B) except that substrate 290A is an SOI substrate which includes a BOX layer 290B. There is no blanket subcollector 255 (see FIG. 7B).

[0057] It should be noted that the second and third bipolar junction transistors 200B and 200C may also be fabricated on an SOI substrate instead of the bulk substrate illustrated in FIGs. 8B and 9B respectively.

[0058] FIG. 11A is a plan view of a fifth bipolar junction transistor suitable for use in an ESD trigger and power clamp circuit according to the present invention and FIG. 11B is a cross-sectional view through line 11B–11B of FIG. 11A. In FIGs. 11A and 11B, a fifth bipolar junction transistor 200E is similar to first bipolar junction transistor 200A (see FIGs. 7A and 7B) except that in FIGs. 11A and 11B a tuning ion implant 295 has been performed to change the doping level of n-well 205 between base 220 and masked subcollector 245. Thus a third tuning of the BV_{ceo} (and f_T) of fifth bipolar junction resistor 200E may be obtained by controlling the ion species, dose and energy of ion–

implant 295.

[0059] It should be noted that the second, third and fourth bipolar junction transistors 200B (see FIGs. 8A and 8B), 200C (see FIGs. 9A and 9B) and 200D (see FIGs. 10A and 10B) may also employ a tuning ion implant as illustrated in FIG. 11B and described supra.

[0060] FIG. 12A is a plot illustrating the relationship between BV_{ceo} and masked subcollector pull back according to the present invention. Curve 60 is based on experimental measurement of BV_{ceo} on NPN SiGe bipolar transistors identical processes and structures except for the amount of masked subcollector pullback on transistors having a total length of about 2.5 microns as measured, for example, between deep trench isolation 155 in FIG. 2B. Curve 60 illustrates that BV_{ceo} can be increased and tuned and significantly.

[0061] FIG. 12B is a plot illustrating the relationship between f_T and masked subcollector pull back according to the present invention. Curve 70 is based on experimental measurement of f_T on the same NPN SiGe bipolar transistors measured to generate curve 60 of FIG. 12A.

[0062] The SiGe bipolar transistors illustrated in FIGs. 2A and 2B, 3A and 3B, 4A and 4B, 5A and 5B, and 6A and 6B and the

bipolar junction transistors illustrated in FIGS. 7A and 7B, 8A and 8B, 9A and 9B, 10A and 10B, and 11A and 11B and described supra, are utilized by the various embodiments of the present invention as trigger or clamp transistors in Darlington type ESD networks as illustrated in FIGs. 13 through 17 and described infra.

[0063] FIG. 13 is an ESD trigger and power clamp circuit according to a first embodiment of the present invention. In FIG. 13, circuit 300 includes transistors T1 and T2 and resistors R1 and R2. The collectors of transistor T1 and T2 are coupled to a VDD power rail and the emitters of transistors T1 and T2 are coupled to a VSS power rail through resistors R1 and R2 respectively. The emitter of transistor T1 is coupled to the base of transistor T2 and the base of transistor T1 is open. Transistor T1 may be selected from any of the SiGe bipolar transistors illustrated in FIGs. 2A and 2B, 3A and 3B, 4A and 4B, 5A and 5B, and 6A and 6B and the bipolar junction transistors illustrated in FIGS. 7A and 7B, 8A and 8B, 9A and 9B, 10A and 10B, and 11A and 11B and described supra. The crooked arrow pointing from the collector to the emitter of transistor T1 indicates transistor T1 has a masked subcollector and that the BV_{ceo} of transistor T1 has been tuned by at least by fixing

the masked subcollector pull back distance as described supra. Transistor T1 may also be further tuned by control of the depth and doping level of the masked subcollector and/or by additional ion implantations between the base and masked subcollector. It should be apparent that the BV_{ceo} tuning is fixed during fabrication of transistor T1. The fact that transistor T1 is a BV_{ceo} tunable bipolar transistor and has a higher BV_{ceo} than would otherwise be obtained, imparts to circuit 300 a higher trigger voltage than would otherwise be obtained using standard bipolar transistors. In a first example the BV_{ceo} of transistor T1 is greater than the BV_{ceo} of transistor T2. In a second example the BV_{ceo} of transistor T1 is less than the BV_{ceo} of transistor T2.

[0064] FIG. 14 is an ESD trigger and power clamp circuit according to a second embodiment of the present invention. In FIG. 13, circuit 305 includes transistors T3 and T4 and resistors R3 and R4. The collectors of transistor T3 and T4 are coupled to a VDD power rail and the emitters of transistors T3 and T4 are coupled to a VSS power rail through resistors R3 and R4 respectively. The emitter of transistor T3 is coupled to the base of transistor T4 and the base of transistor T3 is open. Transistor T4 may be selected from

any of the SiGe bipolar transistors illustrated in FIGs. 2A and 2B, 3A and 3B, 4A and 4B, 5A and 5B, and 6A and 6B and the bipolar junction transistors illustrated in FIGS. 7A and 7B, 8A and 8B, 9A and 9B, 10A and 10B, and 11A and 11B and described supra. The crooked arrow pointing from the collector to the emitter of transistor T4 indicates transistor T4 has a masked subcollector and that the BV_{ceo} of transistor T4 has been tuned by at least by fixing the masked subcollector pull back as described supra. Transistor T4 may also be further tuned by control of the depth and doping level of the masked subcollector and/or by additional ion implantations between the base and masked subcollector. It should be apparent that the BV_{ceo} tuning is fixed during fabrication of transistor T4. The fact that transistor T4 is a BV_{ceo} tunable bipolar transistor and has a higher BV_{ceo} than would otherwise be obtained, imparts to circuit 305 a higher clamping voltage than would otherwise be obtained using standard bipolar transistors. In a first example the BV_{ceo} of transistor T3 is greater than the BV_{ceo} of transistor T4. In a second example the BV_{ceo} of transistor T3 is less than the BV_{ceo} of transistor T4.

[0065] FIG. 15 is an ESD trigger and power clamp circuit accord-

ing to a third embodiment of the present invention. In FIG. 15, circuit 310 includes transistors T5 and T6 and resistors R5 and R6. The collectors of transistor T5 and T6 are coupled to a VDD power rail and the emitters of transistors T5 and T6 are coupled to a VSS power rail through resistors R5 and R6 respectively. The emitter of transistor T5 is coupled to the base of transistor T6 and the base of transistor T5 is open. Transistors T5 and T6 may be independently selected from any of the SiGe bipolar transistors illustrated in FIGs. 2A and 2B, 3A and 3B, 4A and 4B, 5A and 5B, and 6A and 6B and the bipolar junction transistors illustrated in FIGS. 7A and 7B, 8A and 8B, 9A and 9B, 10A and 10B, and 11A and 11B and described supra. The crooked arrow pointing from the collectors to the emitters of transistors T5 and T6 indicates transistors T5 and T6 have masked subcollector and that the BV_{ceo} 's of transistors T5 and T6 have been tuned by at least by fixing the masked subcollector pull back as described supra. Transistors T5 and T6 may also be further tuned by control of the depth and doping level of their respective masked subcollectors and/or by additional ion implantations between their respective bases and masked subcollectors. It should be apparent that the BV_{ceo} tuning is

fixed during fabrication of transistors T5 and T6 and need not be the same for both. The fact that transistors T5 and T6 are BVceo tunable bipolar transistors and have higher BVceo's than would otherwise be obtained imparts to circuit 310 a higher trigger voltage and a higher clamping voltage than would otherwise be obtained using standard bipolar transistors. In one example the BVceo of transistor T5 is less than the BVceo of transistor T6.

[0066] FIG. 16 is an ESD trigger and power clamp circuit according to a fourth embodiment of the present invention. In FIG. 16, circuit 315 includes transistors T7 and T8, resistors R7 and R8 and a varactor V1 comprised of one or more diode elements which may include but is not limited to SiGe base Schotky diodes, complimentary metal-oxide silicon (CMOS) diodes, a SiGe bipolar transistor configured as a diode or a bipolar junction diode configured as a diode. The collectors of transistor T7 and T8 are coupled to a VDD power rail and the emitters of transistors T7 and T8 are coupled to a VSS power rail through resistors R7 and R8 respectively. The emitter of transistor T7 is coupled to the base of transistor T8 and the base of transistor T7 is open. Transistor T7 may be selected from any of the SiGe bipolar transistors illustrated in FIGs. 2A and 2B, 3A

and 3B, 4A and 4B, 5A and 5B, and 6A and 6B and the bipolar junction transistors illustrated in FIGS. 7A and 7B, 8A and 8B, 9A and 9B, 10A and 10B, and 11A and 11B and described supra. The crooked arrow pointing from the collector to the emitter of transistor T7 indicates transistor T7 has a masked subcollector and that the BV_{ceo} of transistor T7 has been tuned by at least by fixing the masked subcollector pull back as described supra. Transistor T7 may also be further tuned by control of the depth and doping level of the masked subcollector and/or by additional ion implantations between the base and masked subcollector. It should be apparent that the BV_{ceo} tuning is fixed during fabrication of transistor T7. The fact that transistor T7 is a BV_{ceo} tunable bipolar transistor and has a higher BV_{ceo} than would otherwise be obtained, imparts to circuit 320 a higher trigger voltage than would otherwise be obtained using standard bipolar transistors. Further, the inclusion of varactor V1 adds additional trigger range outside of the range of transistor T7. For example, if varactor V1 includes 1, 2 or 3 Schotky diodes, the trigger voltage of circuit 315 will be 0.9, 1.2 or 1.5 volts respectively plus the BV_{ceo} of transistor T7. In a first example the BV_{ceo} of transistor T7 is greater than the BV_{ceo}

of transistor T8. In a second example the BV_{ceo} of transistor T7 is less than the BV_{ceo} of transistor T8.

[0067] FIG. 17 is an ESD trigger and power clamp circuit according to a fifth embodiment of the present invention. In FIG. 17, circuit 320 includes transistors T9 and T10, resistors R9 and R10 and a varactor V2 comprised of one or more diode elements which may include but is not limited to SiGe base Schotky diodes, complimentary metal-oxide silicon (CMOS) diodes, a SiGe bipolar transistor configured as a diode or a bipolar junction diode configured as a diode. The collectors of transistor T9 and T10 are coupled to a VDD power rail and the emitters of transistors T9 and T10 are coupled to a VSS power rail through resistors R9 and R10 respectively. The emitter of transistor T9 is coupled to the base of transistor T10 and the base of transistor T9 is open. Transistor T10 may be selected from any of the SiGe bipolar transistors illustrated in FIGs. 2A and 2B, 3A and 3B, 4A and 4B, 5A and 5B, and 6A and 6B and the bipolar junction transistors illustrated in FIGS. 7A and 7B, 8A and 8B, 9A and 9B, 10A and 10B, and 11A and 11B and described supra. The crooked arrow pointing from the collector to the emitter of transistor T10 indicates transistor T10 has a masked subcollector and that the BV_{ceo} of

transistor T10 has been tuned by at least by fixing the masked subcollector pull back as described supra. Transistor T10 may also be further tuned by control of the depth and doping level of the masked subcollector and/or by additional ion implantations between the base and masked subcollector. It should be apparent that the BV_{ceo} tuning is fixed during fabrication of transistor T10. The fact that transistor T10 is a BV_{ceo} tunable bipolar transistor and has a higher BV_{ceo} than would otherwise be obtained, imparts to circuit 320 a higher trigger voltage than would otherwise be obtained using standard bipolar transistors. Further, the inclusion of varactor V1 adds additional trigger range outside of the range of transistor T10. For example, if varactor V2 includes 1, 2 or 3 Schotky diodes, the trigger voltage of circuit 320 will be 0.9, 1.2 or 1.5 volts respectively plus the BV_{ceo} of transistor T10. In a first example the BV_{ceo} of transistor T9 is greater than the BV_{ceo} of transistor T10. In a second example the BV_{ceo} of transistor T9 is less than the BV_{ceo} of transistor T10.

[0068] FIG. 18 is an ESD trigger and power clamp circuit according to a sixth embodiment of the present invention. In FIG. 18, circuit 325 includes transistors T11 and T12, re-

sistors R11 and R12 and a varactor V3 comprised of one or more diode elements which may include but is not limited to SiGe base Schotky diodes, complimentary metal-oxide silicon (CMOS) diodes, a SiGe bipolar transistor configured as a diode or a bipolar junction diode configured as a diode. The collectors of transistor T11 and T12 are coupled to a VDD power rail and the emitters of transistors T11 and T12 are coupled to a VSS power rail through resistors R11 and R12 respectively. The emitter of transistor T11 is coupled to the base of transistor T12 and the base of transistor T11 is open. Transistors T11 and T12 may be independently selected from any of the SiGe bipolar transistors illustrated in FIGs. 2A and 2B, 3A and 3B, 4A and 4B, 5A and 5B, and 6A and 6B and the bipolar junction transistors illustrated in FIGS. 7A and 7B, 8A and 8B, 9A and 9B, 10A and 10B, and 11A and 11B and described supra. The crooked arrow pointing from the collectors to the emitters of transistors T11 and T12 indicates transistors T11 and T12 have masked subcollectors and that the BV_{ceo} 's of transistors T11 and T12 have been tuned by at least by fixing the masked subcollector pull back as described supra. Transistors T11 and T12 may also be further tuned by control of the depth and

doping level of their respective masked subcollectors and/or by additional ion implantations between their respective bases and masked subcollectors. It should be apparent that the BV_{ceo} tuning is fixed during fabrication of transistors T11 and T12. The fact that transistors T11 and T12 are BV_{ceo} tunable bipolar transistors and have higher BV_{ceo} 's than would otherwise be obtained, imparts to circuit 325 a higher trigger voltage and a higher clamping voltage than would otherwise be obtained using standard bipolar transistors. Further, the inclusion of varactor V3 adds additional trigger range outside of the range of transistor T11. For example, if varactor V3 includes 1, 2 or 3 Schotky diodes, the trigger voltage of circuit 325 will be 0.9, 1.2 or 1.5 volts respectively plus the BV_{ceo} of transistor T11. In one example the BV_{ceo} of transistor T11 is less than the BV_{ceo} of transistor T12.

[0069] FIG. 19 is an ESD protection circuit according to a seventh embodiment of the present invention. In FIG. 330 ESD protection circuit includes a pad 335, a circuit 340, a transistor T13 and a resistor R13. Pad 335 is coupled to circuit 340 and the collector of transistor T13. The base of transistor T13 is coupled to ground through optional resistor R13 and the emitter of transistor T13 is coupled to

ground. The crooked arrow pointing from the collector to the emitter of transistors T13 indicates transistor T13 has a masked subcollectors and that the BV_{ceo} 's of transistor T13 have been tuned by at least by fixing the masked subcollector pull back as described supra. Transistor T13 may also be further tuned by control of the depth and doping level of their respective masked subcollectors and/or by additional ion implantations between their respective bases and masked subcollectors. It should be apparent that the BV_{ceo} tuning is fixed during fabrication of transistor T13.

[0070] Traditionally, ESD designs are custom designed using graphical systems. ESD ground-rules and structures are typically built into the designs requiring a mandatory custom layout. An ESD CAD system has been developed to fulfill the objective of design flexibility, RF characterization and models of ESD elements, automation, and choice of ESD network type. This system is fully described in a paper "A Design System for Auto-generation of ESD Circuits," presented at the "International Cadence Usergroup Conference, held Sept 16-18, 2002 in San Jose Ca and is hereby incorporated by reference. The present invention describes a method of designing ESD circuits utilizing

tunable SiGe bipolar and tunable bipolar junction transistors as described supra using this auto ESD circuit generation system with some modification.

[0071] The design system is a hierarchical system of parameterized cells, which are constructed into higher-level ESD networks. Lowest order p-cells are RF and dc characterized. ESD verification, dc characterization, schematics and LVS are completed on the higher order circuits. Diode, bipolar and MOSFET hierarchical cells are used to establish both CMOS MOSFET-based ESD networks and SiGe bipolar-based networks. The parameterized cells, known as P-cells, are constructed in a CADENCETM design system. The p-cells are grow-able elements, which fix some variables, and pass some variables to the higher order circuit through "inheritance". From base p-cells, ESD circuits are constructed for input pads, V_{DD} -to- V_{SS} power clamps, and V_{SS} -to- V_{SS} power clamps. In these categories, there exists both the CMOS-based and the BiCMOS SiGe-based implementations.

[0072] The ESD design system allows for change of circuit topology as well as structure size in an automated fashion. Layout and circuit schematics are auto-generated with the user varying the number of elements in the circuit. The

circuit topology automation allows for the user to auto-generate new ESD circuits and ESD power clamps without additional design work. Interconnects and wiring between the circuit elements are also auto-generated.

[0073] FIG. 20 is a process flow diagram for an exemplary system for designing ESD trigger and power clamp circuits according to the present invention. To achieve auto-generation of ESD circuits the design flow illustrated in FIG. 20 is utilized. A graphical interface 400 allows input to both a schematic P-cell circuit generation module 405 and a hierarchical P-cell layout generation module 410. Schematic P-cell circuit generation module 405 supplies P-cells to a library generation module 415, a circuit generation module 420 and a circuit simulation module 425. Both schematic P-cell circuit generation module 405 and hierarchical P-cell layout generation module 410 supply input into a verification module 430.

[0074] The flow illustrated in FIG. 20 is based on the development of P-cells for both the schematic and layout cells. The P-cells are hierarchical and built from device primitives, which have been RF characterized and models. Without the need for additional RF characterization, the design kit development cycle is compressed.

[0075] FIG. 21 is an exemplary illustration of a GUI screen of the ESD circuit design system illustrated in FIG. 20. In FIG. 21, GUI 435 includes a cell name input field 440, a BV_{ceo} desired value input field 445, a f_T display field 450, a desired trigger voltage input field 455, a transistor length input field 460 and a transistor width input field. After a user fills in all input fields, tunable BV_{ceo} transistors that will meet the inputted criteria are selected from lookup tables of length, width, BV_{ceo} and f_T and an ESD Trigger/Clamp circuit designed using those elements. The f_T is displayed, so the user can make changes if the value of f_T is too low.

[0076] FIG. 22 is an exemplary ESD trigger and power clamp circuit hierarchal structure generated by the ESD circuit design system of FIG. 20. In FIG. 22, the structure for ESD circuits of the type illustrated in FIGs. 13, 14, 15, 16, 17, 18 and 19 and described supra is illustrated. In FIG. 22, a hierarchical P-cell 470 of the ESD power clamp circuit is generated allowing for different sizes. In hierarchical ESD trigger/clamp circuit P-cell 470, the design includes a ballast resistor P-cell 475 and a BV_{ceo} tunable transistor P-cell 480 (or a standard transistor) that make up a clamp P-cell 485 and a bias resistor P-cell 490 and a BV_{ceo} tun-

able transistor P-cell 505 (or a standard transistor) that that make up a trigger P-cell 500. The ESD trigger/clamp circuits of FIGs. 13, 14, 15, 16, 17 and 18 would utilize the P-cells so far described. To address the different power supply conditions trigger P-cell 500 may include a level-shifting parameterized sub-design P-cell 505. The ESD trigger/clamp circuits of FIGs. 16, 17 and 18 would utilize is option.

[0077] Thus the present invention provides an ESD trigger and power clamp circuit compatible with high performance bipolar technology by providing ESD trigger and power clamp circuits incorporating high performance bipolar devices with tunable BV_{ceo} and f_T .

[0078] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. For example, while NPN bipolar transistors have been illustrated and described one of ordinary skill in the art would understand that the present invention is appli-

cable to PNP bipolar transistors as well. Therefore, it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.